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METHOD AND APPARATUS FOR SKEW COMPENSATION

Inventor:

Robert L. Glenn

Neil P. Kelly

Prepared by:
Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8598

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Method and Apparatus For Skew Compensation

FIELD OF THE INVENTION

The field of invention relates to data signal processing generally; and more specifically, to compensating for the skew that exists between a clock signal and a data signal.

BACKGROUND

Figure 1 shows a pair of semiconductor chips 101, 102 coupled together by a serial link 110 having a data signal line 103 and a clock signal line 104. The transmitting unit 101 sends a tx data signal 105 to the receiving unit 102 along tx data signal line 103. The receiving unit 102 uses a tx clock signal 106 that is sent along tx clock signal line 104 to receive the tx data 105.

That is, in the example of Figure 1, the receiving unit 102 clocks the tx data signal 105 on the rising edge of the tx clock signal 106. The tx clock signal 106 may be referred to as a quadrature clock because the phase of its rising edges are 90 degrees away from the rising edges of the tx data signal 105 (using the tx data signal 105 as a phase reference).

A problem with serial links, particularly as their frequency of operation rises, is the presence of skew 109 between a tx data signal 107 and a tx clock signal 108 when it is received at the receiving unit. Skew 109 is any phase relationship between the edges of the tx data signal 107 and tx clock signal 108 other than the nominal or "designed for" phase relationship (such as 90 degrees, using the tx data signal 107 as a phase reference).

Skew may arise because the transfer function and/or trace length of the data signal line 103 is different than the transfer function and/or trace length of the clock signal line 104. For example if the data signal line 103 is shorter or has less capacitance than the clock signal line 103, the rising edges of the tx clock signal 108 will have more than 90 degrees of phase shift with respect to the rising edges of the tx data signal 107.

For a given difference in transfer function and/or trace length between the data and clock signal lines 103, 104, greater skew is observed between the tx data signal and tx data signal as the frequency of operation of the serial link 110 increases. That is, the differences between the signal lines 103, 104 have an effect on the delay of the signals as they propagate from the transmitting unit 101 to the receiving unit 102. As the frequency of the serial link's operation rises, the delay represents a greater percentage of the data signal's pulse widths.

As skew 109 increases the performance of the serial link degrades. That is, because the receiving unit 102 uses the tx clock signal to clock the reception of the data carried by the tx data signal 107, the "misposition" of the tx clock signal 108 edges causes the receiving unit 102 to occasionally clock incorrect data.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the Figures of the accompanying drawings in which:

Figure 1 shows a serial interface;

Figure 2 shows an apparatus that compensates for skew between a data signal and a clock signal;

Figure 3 shows a portion of a transmitting unit having programmable delay units along the tx data signal path and the tx clock signal path;

Figure 4 shows an embodiment for the programmable delay unit of Figure 3; and

Figure 5 shows an embodiment for a transmitting unit having a programmable phase interpolator.

DETAILED DESCRIPTION

A method is described that measures a skew between a data signal and a clock signal at a receiving end of a serial link and then adjusts a phase relationship between the data signal and the clock signal to reduce the skew. An apparatus is described that includes a transmitting unit coupled to a receiving unit by a serial link where the serial link is configured to transport a clock signal and a data signal. The apparatus also includes a skew measurement unit that is coupled to the serial link such that the coupling of the skew measurement unit is closer to the receiving unit than the transmitting unit. A skew adjustment unit is also coupled to the skew adjustment and the transmitting unit.

Figure 2 shows a solution to the skew problem presented in the background. In the approach of Figure 2 the skew between a clock signal and data signal, as it appears when observed proximate to the receiving unit 202, is measured by a measurement unit 204 (e.g., an oscilloscope, a network analyzer, a bit error rate tester, a circuit designed to measure skew, etc.).

After the measurement unit 204 measures the skew, the skew is presented to a skew adjustment unit 205. The skew adjustment unit 204 determines a phase relationship between the tx data signal and the rx clock signal within the transmitting unit 201 that will compensate for (i.e., approximately cancel) the skew observed at the receiving unit 202. The skew adjustment unit 204 then implements the proper phase relationship within the transmitting unit 201.

For example, if the skew observed at the receiving unit 202 corresponds to +2 degrees of phase shift (e.g., the tx clock is shifted by 92 degrees with respect to the tx data signal) the skew adjustment unit 204 programs the transmitting unit

201 to effectively install a difference between the delay experienced by the tx data signal and the delay experienced by the rx data signal as they are processed within the transmitting unit 201.

The difference in delay should correspond (or approximately correspond) to a –2 degree phase shift of the tx clock signal with respect to its nominal phase position. That is, whereas a typical transmitting unit 101 transmits a quadrature tx clock signal at a +90 degree phase shift with respect to the tx data signal discussed in the background and seen in Figure 1, the transmitting unit 201 of Figure 2 is programmed by the skew adjustment unit 204 to transmit a quadrature tx clock signal having a +88 degree phase shift with respect to the tx data signal.

The skew adjustment unit 204 may be any device that determines the proper programmable phase adjustment settings in light of the skew measured by the skew measurement unit 204. The skew adjustment unit may include a centralized processing unit (CPU) that executes a software program configured to the proper adjustment settings. This includes a stand alone personal computer (PC), an electrical circuit board having a CPU, etc. The skew adjustment settings may also be determined and programmed by an individual rather than automated with a CPU and software.

In an embodiment, the transmitting unit 201 and the receiving unit 202 are implemented within different semiconductor chips. In various embodiments, the transmitting unit 201, the receiving unit 202, the measurement unit 204 and/or the skew adjustment unit 205 may be integrated together on the same semiconductor chip in various combinations. For example, all four units 201, 202, 204, 205 may be integrated together on the same chip. Alternatively, as another example, the

skew measurement unit 204 may be integrated onto the same semiconductor chip with the receiving unit 202 and the skew adjustment unit 204 may be integrated onto a different semiconductor chip with the transmitting unit 201.

In an alternate embodiment, rather than measure the skew observed at the receiving unit 202, a favorable tx data signal/rx data signal phase relationship is known for the receiving unit 202. For example, if it is known that the receiving unit 202 operates better if a –2 degree skew (i.e., +88 degree phase relationship) exists at its input (e.g., because of different delays internal to the receiving unit 202 for the two signals), the transmitting unit 201 is programmed by the skew adjustment unit 204 to transmit a quadrature tx clock signal at a –2 degree skew (i.e., a +88 degree phase relationship).

The favorable phase relationship may be provided by the manufacturer of the receiving unit 202. In a further embodiment, both approaches discussed above are simultaneously employed. That is, the transmitting unit 201 is programmed according to both measurement data taken by the measurement unit 204 and a known phase relationship favored by the receiving unit 202

For example if the receiving device favors a –2 degree skew (i.e., a +88 degree phase relationship) and a +2 degree skew (i.e. +92 degree phase relationship) is observed by the measurement unit 204 when the transmitting unit 201 is transmitting at a 0 degree skew (i.e., +90 degree phase relationship), the skew adjustment unit 205 programs the transmitting unit 201 to transmit the tx data signal and tx clock signal at a –4 degree skew (i.e., a +86 phase relationship). In this case, the skew adjustment compensates for both the +2 skew associated

with the signal lines between the chips 201, 202 and the –2 skew associated with the phase relationship favored by the receiving unit 201.

Figure 3 shows an embodiment of a design 301 that may be used within the transmitting unit 201 of Figure 2 to adjust the skew of a tx data signal and a tx clock signal. A pair of programmable delay units 304, 305 are positioned prior to line drivers 302, 303. A programmable delay unit will impart an amount of delay on a input signal based upon the value of a skew adjustment input word.

Thus programmable delay unit 304 imparts a delay upon the data signal based upon the value of the data skew adjustment word and programmable delay unit 305 imparts a delay upon the quadrature clock signal based upon the value of the clock skew adjustment word. The skew between the tx data signal and the tx clock signal is a function of the difference in delay experienced by the signals through their respective programmable delay units 304, 305.

For example if programmable delay unit 304 exerts a 75ps delay on its input data signal and if programmable delay unit 305 exerts a 75ps delay on its input quadrature clock signal, no skew is tailored between the two signals by the programmable delay units. However, if instead programmable delay unit 304 exerts a 75ps delay and programmable delay unit 305 exerts a 100ps delay upon the quadrature clock signal, a –25ps skew is created between the two signals. Line drivers 304, 305 are circuits that are capable of driving the tx data signal and tx clock signal across their respective signal lines to the receiving unit (not shown in Figure 3).

Figure 4 shows an embodiment 404 of a programmable delay unit that includes a cascade of inverters that each have an adjustable propagation delay. In

the embodiment of Figure 4, the input data signal is a differential signal. The differential input signal is presented to the input of a source coupled FET logic (SCFL) inverter stage 410. Inverter stage 410 drives a second inverter stage 420. Further inverter stages may be cascaded from inverter stage 420.

Note that a capacitance C1, C2 is shunted from each signal line that couples the inverter stages 410, 420. Each capacitance C1, C2 is further coupled to ground via a switch S1, S2. The throw of both switches S1, S2 are coupled such that either both switches S1, S2 are open or both switches S1, S2 are closed. If the switches are closed, additional capacitance C1, C2 is added to the signal lines which increases the delay experienced by the data signals. If the switches S1, S2 are open the capacitance C1, C2 has no effect on the delay experienced by the data signals.

Thus, the propagation delay may be controlled by opening and closing a specific number of switch pairs in the cascade of inverter stages. Maximum delay is exerted on the data signals if all switches are closed. Correspondingly, minimum delay is exerted on the data signals if all switches are open. The position of each pair of switches (i.e., open or closed) is determined by the value of a skew adjustment word bit.

For example, if the skew adjustment word bit "A" is a "1" the switches S1, S2 are open while if the skew adjustment word bit "A" is a "0" the switches S1, S2 are closed. The position of each pair of switches within the cascade of inverter stages is controlled by a different skew adjustment word bit. Thus, different delays through the programmable delay unit 404 may be crafted with different skew adjustment word values. In an alternate embodiment, a cascade of inverters

may be employed having a fixed propagation delay where the value of the skew adjustment word controls how many of the inverters the signal flows through. As the signal flows through more inverters, the delay increases (and as the signal flows through less inverters, the delay decreases).

Figure 5 shows another alternative embodiment 500 that provides for programmable skew adjustment. The design of Figure 5 may be used in networking applications to time the clocking of a serial link with a clock located on the transmitting end of a network. That is, for example, the parallel data may be received from a network such as a 1.00 Gb/s Ethernet network and the serial tx data 551 shown as the output of Figure 5 is clocked according to a clock that is effectively received from the data being received on the network.

A network interface such as a physical layer (PHY) presents the serial link circuitry 500 with data received from the network. The PHY formats the data received from the network into a parallel data stream "parallel data" and also provides a receive clock (not shown in Figure 5) that is: 1) extracted from the data received on the network; and 2) properly times the byte-wide data received from the PHY (e.g., a 125Mhz clock for a byte wide of data having a 1 Gb/s data rate). Reference clock 550 ("Ref clock"), in an embodiment, is a local oscillator used as a reference from which a transmit clock for the PHY is derived and from which a serial received clock from the PHY is generated as described in more detail below.

The parallel to serial converter 501 converts the parallel data into serial data (i.e., "serial tx data"). The parallel to serial converter embodiment 501 of Figure 5 employs a double edged transmission approach where a next serial tx data signal 551 value is effectively triggered upon both edges of a data clock

signal 520 cycle. Note that, in the approach of Figure 5, the maximum data rate of the serial tx data signal 551 corresponds to the frequency of the tx clock signal 552 and the data clock signal 520.

That is, for a "101010..." tx data pattern (as seen in Figure 5), a new serial tx data signal 551 value is observed for each edge of the data clock signal 520 (as opposed to half of the edges as seen in Figure 1). This corresponds to a 1.25 Gb/s serial tx data signal 551 for a 625 Mhz data clock signal 520 and tx clock signal 552 (because there are two serial data bits per clock cycle). Note that, in this embodiment, the parallel to serial converter 501 employs an encoding scheme (e.g., 8B/10B or 4B/5B) that effectively boosts the line speed beyond the actual data rate received from the network (e.g., 1 Gb/s data rate is boosted to a 1.25 Gb/s serial tx data signal baud rate).

In the embodiment of Figure 5, the data clock 520 and tx clock 552 are both higher frequencies than the ref clock 550. That is, the ref clock 550 is effectively multiplied by a factor of "K1" by a frequency multiplier 504 before being delivered to a pair of phase interpolator units 502, 503. In an embodiment, frequency multiplier 504 is a phase lock loop circuit.

A phase interpolator is a circuit that can adjust the phase of a signal by 360 degrees or more per second which effectively adds to the frequency of the signal. For example, if a 1kHz signal is provided to a phase interpolator that adds 720 degrees of phase shift to the signal per second, the phase interpolator output corresponds to a 1.002 kHz signal because 720 degrees of phase shift per second corresponds to an extra 2Hz added to the frequency of the signal.

The increase in frequency to the ref clock 550 is provided by operation of the frequency multiplier 504 (which multiplies the ref clock 550 by a fixed amount K1). The pair of phase interpolators 502, 503 adjust the increased frequency by a variable amount depending on the phase interpolator control input 521 (which controls the amount of phase adjustment in units of degrees/sec).

In an embodiment, the phase interpolator control input 521 is controlled by a circuit (not shown in Figure 5 for simplicity) that is coupled to the network line from which the parallel data is first received. Via feedback (which is also not shown in Figure 5 for simplicity) from the output of one or both of the phase interpolators 502, 503, the phase interpolator control input 521 stabilizes when the divided down frequency of the phase interpolator output signals (data clock 520, tx clock 552) approximately "matches" the frequency of the receive data frequency from the PHY (e.g., a 625Mhz interpolator output frequency divided by 5 corresponds to a 125 Mhz PHY receive clock for a byte wide of data having a 1 Gb/s data rate).

As such, the data clock signal 520 and the tx clock signal 552 have a frequency that corresponds to a received clock from the network. A first phase interpolator 502 helps generate the data clock 520 signal used by the parallel to serial converter 501 to time the transmission of the serial tx data 551. The second phase interpolator 503 helps generate the tx clock 552 that is sent along with the serial tx data.

The second phase interpolator 503 has a skew control adjustment 522 that controls an offset between the phase adjustment performed by the first phase

interpolator 502 and the phase adjustment performed by the second phase interpolator 503. For example, referring to the phase diagram 525 of Figure 5, phasor 507 corresponds to the phase adjustment performed by the first phase interpolator 502 and phasor 508 corresponds to the phase adjustment performed by the second phase interpolator 503. The rate of the counter-clockwise spin of the phasors is controlled by the phase interpolator control input 521 (which, again, corresponds to the phase adjustment measured in degrees/sec). Since the rate of both phasors 507, 508 is controlled by the same input 521, the pair of phase interpolators 502, 503 increase the frequency of their corresponding input signals by the same amount.

Note that the phasors 507, 508 have a phase offset of 90 degrees with respect to one another. As a result of this phase offset, the data clock 520 and tx clock 552 (as seen in the waveform diagrams of Figure 5) have a 90 degree phase offset with respect to one another. This sets the proper nominal phase relationship between the serial tx data and the tx clock. This nominal phase difference of 90 degrees may be designed into the phase interpolators 502, 503 themselves (i.e., phase interpolator 503 by design has a 90 degree offset with respect to phase interpolator 502).

The skew control adjustment 522 of the second phase interpolator 503 adjusts this nominal phase offset of its corresponding phasor 508 and, as such; may be used to apply the desired skew between the serial tx data and the tx clock as discussed with respect to Figure 2. The value of the skew control adjustment 522 input may be programmably controlled so that a desired skew can be programmed as discussed above. In a further embodiment, the frequency

multiplier 504 output is "tapped" to generate a local transmit clock for the network PHY.

Note also that embodiments of the present description may be implemented not only within a semiconductor chip but also within machine readable media. For example, the designs discussed above may be stored upon and/or embedded within machine readable media associated with a design tool used for designing semiconductor devices. Examples include a netlist formatted in the VHSIC Hardware Description Language (VHDL) language, Verilog language or SPICE language. Some netlist examples include: a behaviorial level netlist, a register transfer level (RTL) netlist, a gate level netlist and a transistor level netlist. Machine readable media also include media having layout information such as a GDS-II file. Furthermore, netlist files or other machine readable media for semiconductor chip design may be used in a simulation environment to perform the methods of the teachings described above.

Thus, it is also to be understood that embodiments of this invention may be used as or to support a software program executed upon some form of processing core (such as the CPU of a computer) or otherwise implemented or realized upon or within a machine readable medium. A machine readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.